PATENT

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DIGITAL DATA TRANSMISSION SYSTEM WITH
DEVICE FOR CORRECTING BASELINE WANDER

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority from prior European Patent

10 Application No. 00830654.0, filed October 6, 2000, the entire disclosure of which is herein

incorporated by reference.

BACKGROUND OF THE INVENTION

1.   Field of the Invention

The present invention relates to a digital data transmission system (e.g., at

15 100Mb/s) with a device for correcting the baseline wander, and is particularly suited for an

ethernet system. The present invention also relates to a receiver of a digital data

transmission system (e.g., at 100Mb/s).

2.   Description of Related Art

20   Typically, an ethernet system comprises several stations which transmit and receive

data from at least one central hub by utilizing fibers or twisted wire pairs as transmission

means. The several stations transmit digital data through the transmission means and both

the stations and the central hub must have suitable transformers for receiving and

transmitting data.

25   In the case where a 100Mb/s data transmission must be achieved (for example

through a category 5 wire twisted pair), a 4-bit or 5-bit encoder can be utilized. The

resulting 125Mb/s binary signal is converted to a three-level transmission signal by utilizing an MLT3 line encoding. Such MLT3 encoding results in a base band signal that consists of three levels : +1, 0, -1. A binary signal is transformed into an MLT3 signal by mapping each digital one into a transition and each digital zero into a no transition. For example, a binary series of five ones cause an output which cycles through three levels in the following order: 0, +1, 0, -1, 0.

The non-ideal transmission channel, which comprises the transformers that couple both the stations and the central hub to the transmission means, may cause the waveform of the received signal to be significantly different from the waveform of the transmitted signal. An undesired effect of the transmission channel on the waveform of the transmitted signal is commonly called "baseline wander". To minimize the tones in the transmitted spectrum, the digital data are scrambled prior to being encoded according to MLT3 encoding. In the worst case, the output of the scrambler may have up to 56 consecutive zeroes.

The scrambled digital signal is MLT3 encoded and it is then coupled for example to a category 5 wire twisted pair through transformers. Since the transformers are high pass filters in nature, the energy below their cutoff frequency of about 50 kHz is lost. If in the signal many periods with few transitions are present, the signal loses significantly energy at low frequencies due to the presence of the transformer. In this way, the received waveform can suffer clipping within the receiver and induce errors in the received data even in the case where the lengths of the lines are short. For this reason, the baseline wander effect must be correct in the receiver.

One recent solution allows recovery of data through data slicers, that is elements able to recover data in the receiver and which allow by means of a digital-analog converter to add the information of the low frequency component to the input of the receiver, as described in the article "A CMOS Transceiver for 10-Mb/s and 100-Mb/s ethernet" (IEEE Journal of Solid-state Circuits, Vol. 33, No. 12, December 1998, pages 2169-2177).

SUMMARY OF THE INVENTION

In view of these drawbacks, it is an object of the present invention to overcome the above-mentioned drawbacks and to provide an improved digital data transmission system with a device for correcting the baseline wander.

5   According to preferred embodiments of the present invention, there is provided a digital data transmission system comprising at least one unit which transmits a first MLT3 signal which contains the digital data over at least one cable, at least one second unit which receives the first MLT3 signal and recovers the digital data and transformers which uncouple the at least one first and second unit from the cable, the at least one second unit

10   comprising an equalizer which receives in input the first MLT3 signal and produces a second MLT3 signal in output which is in turn in input to a recovery module for the transmitted digital data, characterized in that the at least one second unit comprises a device placed in feedback to the equalizer, the device receiving in input the second MLT3 signal and producing in output a third low frequency signal which can be added to the first MLT3

15   signal at the input of the equalizer, the device comprising a block designated for the up or down or no translation of the second MLT3 signal according to the respective low or high or intermediate value of such signal and a low pass filter which receives the signal in output from the translation block and produces in output the third signal which contains the low frequency component of the second MLT3 signal.

20   The present invention also provides a receiver of a digital data transmission system.

The present invention makes it possible to form a digital data transmission system with a device for correcting of the baseline wander which makes such correction in analog way and in a more exact and stronger way for the presence of the analog feedback.

Other objects, features, and advantages of the present invention will become

25   apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of

the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

5   Figure 1 is a scheme for a digital data transmission ethernet system according to one embodiment of the present invention;

Figure 2 is a circuit scheme of a receiver of the digital data transmission ethernet system of Figure 1 with a device for correcting the baseline wander according to a preferred embodiment of the present invention;

10   Figure 3 is a timing diagram of the ideal waveform of the input voltage of the receiver;

Figure 4 is a timing diagram of the ideal waveform of the input voltage of the equalizer of Figure 2;

Figures 5-9 are timing diagrams of the voltages in several points of the circuit which

15   derive from simulations over an ethernet system of the type of Figure 1 with a cable of 100m;

Figures 10-12 are eye diagrams of the transmitted, received and corrected voltages derived from simulations over an ethernet system of the type of Figure 1 with a cable of 100m; and

20   Figure 13 is a circuit scheme of a receiver of the digital data transmission ethernet system of Figure 1 with a device for correcting the baseline wander according to another embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

25   Preferred embodiments of the present invention will be described in detail hereinbelow with reference to the attached drawings.

In Figure 1, a 100Mb/s digital data transmission ethernet system is schematically shown. The system comprises an unit 100 for transmitting digital data transformed into a MLT3 voltage signal V(TX), that is a voltage signal that consists of three levels : +1, 0, -1 wherein each digital one is mapped into a transition and each digital zero is mapped into a no transition. Such signal V(TX) is sent from the unit 100 by means of a first transformer 1 through a cable 2 with a length of 100m which is constituted of a category 5 twisted wire pair.

By means of a second uncoupling transformer 3 the signal is received by a receiver 4 shown in more detail in Figure 2. The received signal inR (which is the input current signal of a resistor R) is attenuated, distorted and affected by the phenomenon of the baseline wander (when in the signal many periods with few transitions are present) because the transformers 1 and 3 operate as high pass filters with a cutoff frequency of about 50 kHz.

The signal inR is added to a signal Dv, which is the voltage signal constituted by the current signal Iblw for the resistor R, to achieve the voltage signal inE. The signal Iblw is the feedback signal generated by a device 5 for correcting the baseline wander. Such device comprises a comparator 6, switches 7-9 controlled by the output signal of the comparator 6 and a low pass filter 10. The switches 7 and 9 are connected to two direct voltage generators, respectively V1 at 1V and V2 at -1V. The voltage signal inE is input to an equalizer 11 which produces an output signal outE. Such signal is supplied both to the comparator 6 and to the switches 7-9. According to the voltage value of the signal outE, (that is if such signal is lower than -0.5V, between -0.5V and 0.5V, or higher than 0.5V), the signal outE is translated or is not translated in voltage, and specifically it is translated in voltage of 1V, is not translated or is translated in voltage of -1V.

The signal inLP so-achieved is supplied to the low pass filter 10 having a cutoff frequency of about 50 kHz. The voltage signal output from the filter 10 controls a current generator I(V) which produces the current signal Iblw directly proportional to the voltage output from the filter 10. In this way, the direct component lost in the two transformers 1

and 3 is recovered. The block between the nodes where it is possible to detect the signals inR and outE has a transfer function equal to that of a high pass filter having a zero in the origin and the first pole at about 500 kHz. The output signal outE is also similar to the transmitted signal and it is sent to a transmitted digital data recovery block 20. It is possible to use a uncoupling buffer 300 between the output of the equalizer and the switches.

In Figures 3 and 4, the ideal waveform of the signals inR and inE in the event where bit sequences with 56 zeroes and 4 ones are transmitted (the ones are indicated by signal transitions and the zeroes by no signal transitions). The effect of the baseline wander, which is not present in the signal inE for the correction operated by the device 5, can be shown in the signal inR.

In Figures 5-9, timing diagrams of the voltages at several points of the circuit which derive from simulations over an ethernet system of the type of Figure 1 with a cable of 100m are shown. The transmitted voltage signal V(TX) (Figure 5) of the MLT3 type is attenuated and distorted by the cable 2 and by the transformers 1 and 3, so that it produces a signal inR (Figure 6) input to the receiver. The current signal Iblw (figure 9), which has a time waveform depending on the characteristic of the low pass filter 10, produces the signal Dv over the resistor R which is added to the signal inR for giving the signal inE (Figure 7) input to the equalizer 11. The signal outE (Figure 8) output from the equalizer 11 is the equalized signal with the recovered direct component.

In the Figures 10-12, eye diagrams of the signal V(TX) (Figure 10), the signal inR (Figure 11) and the signal outE (Figure 12) are shown, with such signals being obtained from simulations over an ethernet system of the type of Figure 1 with a cable of 100m. It is possible to see from the distance among the signal paths in the eye diagram of the signal outE that such signal offers a large action field to the circuits following the device 5 of Figure 2.

In Figure 13, there is shown a circuit scheme of a receiver of the 100Mb/s digital data transmission ethernet system of Figure 1 with a device for correcting the baseline

wander according to another embodiment of the present invention. Such circuit scheme differs from the circuit scheme of Figure 2 in the presence of a voltage/current converter 200 which converts the voltage signal outE output from the equalizer 11 into a current Iout which is supplied both to the comparator 6 and to the switches 7-9 controlled by the comparator 6. Two direct current generators I1 and I2 are respectively connected to the switches 7 and 9, with respective values of 100 µA and -100 µA.

According to the value of the signal Iout, (that is, if such signal is lower than -50 µA, is between -50 µA and 50 µA, or is higher than 50 µA), the signal Iout is translated or is not translated in current, and specifically it is translated in current of 100 µA, is not translated, or is translated in current of -100 µA. The signal IinLP so-achieved is sent in input to the low pass filter 10 having a cutoff frequency of about 50 kHz. The voltage signal output from the filter controls the current generator I(V) which produces the current signal Iblw which is directly proportional to the voltage output from the filter 10.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Furthermore, an embodiment of the present invention may not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.